Module No.	Unit No.	Topics	Hrs.
1.0		**Introduction to FPGA and Synthesis**	**04**
	1.1	Compare FPGA, ASIC, SOC, Basic FPGA architecture, Compare various FPGA Boards**, Understanding VLSI Design flow	
	1.2	**Understanding Tools :** Functional simulation , Synthesis and implementation, Synthesis tool flow, Implementation and bit generation, making User constraint files (UCF)	
	1.3	**Study Material** : https://www.xilinx.com/support/university/ise/ise-workshops/ise-fpga-design-flow.html	
2.0		**Writing First program in Verilog**	**04**
	2.1	**Introduction to Verilog**: Module definition, port declaration, connecting ports, Writing first Testbench	
	2.2	**Exercise :** Program for All gates, Writing Test bench and UCF	
	2.3	**Study Material**: https://www.xilinx.com/support/university/ise/ise-teaching-material/hdl-design.html	
3.0		**Combinational design Using VERILOG**	**08**
	3.1	Gate Level Modelling, hierarchical name referencing, **Data Flow Modelling**: Continuous assignments, delay specification, expressions, operators, operands, operator types	
	3.2	**Exercise:** Programming and FPGA implementation of Adders, 4-bit adders, Mux and decoders, **Interfacing** LED, switches with FPGA	
	3.3	**Study Material :** https://onlinecourses.nptel.ac.in/noc20_cs63/preview	
4.0		**Sequential design Using VERILOG**	**08**
	4.1	**Behavioral Modelling :** Structured procedures, initial and always, blocking 'and non-blocking statements, delay control, event control, conditional statements, multi way branching, loops, sequential and parallel blocks **Advanced topics:** Tasks and Functions, generic programming with parameters.	
	4.1	**Exercise:** Programming and FPGA implementation of Counters FFs and Shift registers Interfacing Seven Segment Display, UART with FPGA	
5.0		**Project Outline**	**08**
	5.1	Clocked Synchronous State-Machine Analysis, State-Machine Structure, Output Logic, Characteristic Equations Analysis of State Machines with D Flip-Flops, Clocked Synchronous State-Machine Design, Designing State Machines Using State Diagrams, State Tables	
	5.2	**Project Design Steps**: Designing state diagram, block diagram of project, Selection of FPGA for project, Selection of synthesis and simulation tool.	
6.0		**Project Implementation and management**	**20**
	6.1	Git Repositories, Learning of Project management software's like CVS, SVN etc	
	6.2	Project Implementation: Verilog coding, simulation, Synthesis, Bit generation and downloading on FPGA. .	
	6.3	Result verification and testing	
		Total	**52**